PATENT

Amendments to the Specification

Please replace paragraph [0023] with the following amended paragraph in which added matter is underlined and deleted matter is shown using ~~strikethrough~~:

[0023] The output of the OTA 205 is coupled to the non-inverting input of the error amplifier 111. The inverting input and the output of the error amplifier ~~121~~ 111 are coupled to external pins P2 and P3, respectively. A user selects and couples a compensation resistor RC and a compensation capacitor CC in series between pins P2 and P3 to provide compensation for the error amplifier 111 as known to those skilled in the art. The user also couples the output sense circuit 103 between pin P2 and VOUT to enable feedback sensing of the VOUT signal. In the embodiment shown, the output sense circuit 103 includes a first resistor RA coupled between pin P2 and ground and a second resistor RB between pin P2 and the PWM DC-DC converter output voltage VOUT. In this case, the resistors RA and RB form a voltage divider that develops the VOFB signal as a portion of the VOUT signal, where the VOFB signal is provided to the inverting input of the error amplifier 111. The resistive values of RA and RB are selected by the user to divide the voltage of VOUT to a suitable voltage level at pin P2 to enable the controller 101 to control or otherwise regulate the voltage level of VOUT to a selected level based on VREF. In the configuration shown, the resistance values of RA and RB are selected to develop a voltage level at pin P2 substantially equal to VREF (e.g., 0.6 V) when VOUT is at the target voltage level.

Please replace paragraph [0032] with the following amended paragraph in which added matter is underlined and deleted matter is shown using ~~strikethrough~~:

[0032] If and when the OCP signal is asserted while in state S2, operation returns to state S0 in which the A and C signals are once again asserted high to turn switches 213 and 217 back on and the B signal is pulled low to turn off switch 215. The capacitor 219 is again discharged and operation remains in state S0 until the SSCAP falls below VMIN. The SSEN signal is negated so that the GCL 107 once again disables switching of Q1 and Q2. Once set, the OCP signal (or flag) remains asserted until reset in state S1. The CNT value of the counter 229 is initially zero. After SSCAP falls below VMIN, while OCP is

set and while the CNT value of the counter 229 is not equal (where "!=" denotes inequality) to a predetermined count value CV (e.g., CV = 3 or any other suitable count value), operation proceeds to state S3 in which the C signal is asserted low to turn off the switch 217. The OTA 205, in the open loop configuration, begins charging the capacitor 219 again and operation remains in state S3 while the SSCAP signal is less than a predetermined voltage level, such as VREF, as indicated by the CHG signal being low. When the voltage of SSCAP becomes substantially equal to VREF as indicated by assertion of the CHG signal, operation returns to state S0 and the value of the CNT count of the counter 229 is incremented. Operation toggles between states S0 and S3 in this manner multiple times until the CNT value of the counter ~~129~~ 229 reaches the predetermined count value CV. After SSCAP falls below VMIN, if the ENABLE signal is asserted, the OCP flag is set and if the count value equals the predetermined count value CV, operation proceeds to state S1, where the OCP signal is negated (or the OCP flag is cleared) and the CNT value of the counter 229 is also cleared. The counter 229 and the toggling between states S0 and S3 establish a start-up wait period defined as CV times the time it takes for SSCAP to charge to VREF. In the embodiment shown, the OTA 205 provides a current of approximately 30 microamperes (μA) and the size of the capacitor 219 is selected by the user.